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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/820,898	03/30/2001	Girish P. Ramanathan	219.39304X00	4441

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EXAMINER	
DU, THUAN N	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 09/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/820,898	RAMANATHAN ET AL.	
	Examiner	Art Unit	
	Thuan N. Du	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 May 2004 and 22 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,8,9 and 13-15* is/are rejected.

7)☒ Claim(s) *4-7 and 10-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendments (dated 5/28/04 and 7/22/04).

2. Claims 1-15 are presented for examination.

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Drawings

4. The drawings were received on 7/22/04. These drawings are accepted.

Claim Objections

5. Claims 4 and 10 are objected to because of the following informalities:

In claim 4, line 13, a period (".") at the end of the line is missing.

In claim 10, line 13, a "0" should be deleted.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. Claims 1-3, 8, 9 and 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeddeloh (U.S. Patent No. 6,401,213) in view of Churchill et al. [Churchill] (U.S. Patent No. 6,286,118) (Churchill was cited in previous office action).

7. **Regarding claim 1**, Jeddeloh teaches a method for determining time margins (timing relationship) between strobe (202) and data (204) signals comprising the steps of:

connecting an interface (108) between two chips (102 and 104) [Fig. 1; col. 2, lines 63-64];

providing data (204) and strobe (202) signals from one chip to said interface [Fig. 2; col. 3, lines 3-4, 49-51];

providing a delay in one of said data and strobe signals within said interface [col. 3, lines 62-65]; and

varying said delay over a sequence of instructions [col. 5, lines 21-23, 52-54].

Jeddeloh does not explicitly show the chip(s) having a core and an I/O device. One of ordinary skill in the art would have readily recognized that the chip 102 would include a core portion in order to generating data and strobe signals (handle the main function of the chip)[1] [col. 3, lines 3-4] and an I/O portion in order to communicate with chip 108 (connecting the core portion to other chip(s))[2].

Moreover, Jeddeloh does not explicitly teach the delay is varied over a sequence of instructions to determine when errors occur to indicate the maximum time margin available.

Churchill teaches a method comprising:

providing a delay in a given signal [col. 3, lines 51-53; col. 7, lines 43-46];

varying the delay over a sequence of instructions [col. 7, lines 47-48; Table 2]; and

determining when errors occur and hence the maximum time margin available [col. 7, lines 47-51].

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[1] Defined by applicant at page 2, lines 3-4.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Jeddeloh and Churchill because they both teach method for varying the delay of a signal. Churchill's teaching of varying the delay to determine the timing margins would increase the reliability of Jeddeloh's system by allowing the system accurately measures timing margins to ensure the system will operate properly.

8. **Regarding claim 2**, Jeddeloh does not explicitly show the system having system clock provided to the circuits within the system. One of ordinary skill in the art would have recognized that a system clock of a computing system is normally used as reference clock to the circuits. Therefore, it would have been obvious to one of ordinary skill in the art to recognize that Jeddeloh would include a system clock provided to all circuitries, including circuit 108, within the system in order for the circuitries operate properly and synchronously.

9. **Regarding claim 3**, Jeddeloh teaches the method further comprising:

producing a data sync signal (DAT_SMP 312) from said data signal (DATA 508) and a clock signal (CLK_1 402) [Fig. 5; col. 4, lines 32-50]; and

producing a strobe sync signal (CLK_SMP 310) from said strobe signal (R_STRB 216) and said clock signal (CLK_1 402) [Fig. 5; col. 4, lines 32-50].

10. **Regarding claims 8 and 9**, Jeddeloh and Churchill together teach the claimed method steps. Therefore, Jeddeloh and Churchill together teach the apparatus to implement the claimed method steps.

11. **Regarding claim 13**, Jeddeloh teaches a method for determining timing margining (timing relationship) in a high speed source synchronous interface (108) comprising the steps of:

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[2] Defined by applicant at page 2, lines 4-7.

providing a data signal (DATA 204) [Fig. 2; col. 3, lines 3-4, 49-51];

providing a strobe signal (STROBE 202) [Fig. 2; col. 3, lines 3-4, 49-51];

changing the relationship between said strobe signal and said data signal (delaying the strobe signal) so as to determine the setup and hold of data with respect to strobe [col. 3, lines 7-8, 54-60; col. 5, lines 20-23; col. 5, line 60 to col. 6, line 2].

Jeddeloh does not explicitly teach the relationship between said strobe signal and said data signal is changing in time to detect when failure occurs to indicate the maximum time margin.

Churchill teaches a method comprising:

providing a delay in a given signal [col. 3, lines 51-53; col. 7, lines 43-46];

varying the delay [col. 7, lines 47-48; Table 2]; and

detecting when a failure occurs so as to determine the maximum time margin [col. 7, lines 47-51].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Jeddeloh and Churchill because they both teach method for varying the delay of a signal. Churchill's teaching of varying the delay to determine the timing margins would increase the reliability of Jeddeloh's system by allowing the system accurately measures timing margins to ensure the system will operate properly.

12. **Regarding claim 14**, Jeddeloh teaches the high speed source synchronous interface (108) is arranged between two chips (102 and 104) of a chip set [Fig. 1; col. 2, lines 62-64].

13. **Regarding claim 15**, Jeddeloh teaches that the moving of the strobe signal includes changing a delay of the strobe signal [col. 3, lines 7-8, 57-60, 64-65; col. 5, lines 20-23].

Allowable Subject Matter

14. Claims 6-7 are objected to as being dependent upon a rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

15. Claims 4-5 and 10-12 would be allowable if the minor informalities in the claims have been corrected.

Conclusion

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thuan N. Du whose telephone number is (703) 308-6292 (after 10/14/04, (571) 272-3673). The examiner can normally be reached on Monday-Friday: 9:00 AM - 5:30 PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on (703) 308-1159 (after 10/14/04, (571) 272-3670).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

The fax number for the organization is (703) 872-9306.

Thuan N. Du
September 22, 2004